NONVOLATILE FERROELECTRIC MEMORY DEVICE

Field of the Invention

5   The present invention relates to a nonvolatile ferroelectric random access memory; and, more particularly, to a method for generating a reference voltage in the ferroelectric random access memory of current gain cell mode.

10 ## Description of Related Arts

A ferroelectric random access memory FeRAM, which is nonvolatile ferroelectric memory, has been spotlighted as a memory device of next generation since the FeRAM has a same data processing speed of a dynamic random access memory DRAM and has a nonvolatile characteristic, which preserves data without electric power.

FeRAM has similar structure of DRAM. That is, it is a memory device including a unit cell having 1 transistor 1 capacitor (1T1C) structure, which means the unit cell is constructed with one transistor and one capacitor. Also, FeRAM includes a ferroelectric capacitor in order to use high remnant characteristic of the ferroelectric. By using ferroelectric capacitor, data can be preserved when an electric field is eliminated.

Fig. 1 is a graph showing a characteristic of hysteresis loop of a conventional ferroelectric.

Referring to Fig. 1, although induced polarization eliminates the electric field, the electric field is not eliminated because of existence of remnant and a certain level of the electric field is maintained. The nonvolatile ferroelectric memory cell puts into practical use of a switching charge Q1 and non-switching charge Q0 of the ferroelectric for implementing a memory cell by mapping the Q1 to a logic '1' and the Q0 to a logic '0'.

Fig. 2 is a circuit diagram illustrating a unit cell of conventional ferroelectric memory.

Referring to Fig. 2, the unit cell is formed by including a word line WL and a plate line PL formed in direction of row, a bit line formed in a direction of crossing the word line and plate line, a switching transistor TR having a gate connected to the word line WL, a drain connected to the bit line BL, and a ferroelectric capacitor FC having one end connected to a source of the transistor TR, and another end connected to the plate line PL. A plurality of the above mentioned unit cells is constructed to a cell array unit.

In a mean time, for operating the ferroelectric memory, a reference voltage is required. For reading data stored in the unit cell, a data voltage transmitted to a main bit line BL needs to be compared with the reference voltage transmitted to a sub bit line /BL and to be amplified since the data voltage transmitted to the main bit line is so minute.

Figs. 3A and 3B are circuit diagrams showing a conventional reference cell for generating a reference voltage

in accordance with two different conventional methods.

Referring to Fig. 3A, the reference cell uses two cells having a ferroelectric capacitor, which is identical size of the capacitor in the memory cell, and a mean signal of a cell having data as '1' and other cell having data as '0' is used as a reference signal. In the Fig. 3A, RWL is a word line of the reference cell and RPL is a plate line of the reference cell.

The reference cell shown in Fig. 3A is required to have exact mean value of a cell having data as '1' and other cell having data as '0'. However, it is impossible to provide exact mean value since degradation speeds of switching charge and non-switching charge of the ferroelectric capacitor are different.

For overcoming the above mentioned problem of the reference cell in Fig. 3A, different size of ferroelectric capacitor is used in reference cell of Fig. 3B comparing to a ferroelectric capacitor in a memory cell. It shows method generating non-switching charge as a reference signal by using larger ferroelectric capacitor in the reference cell comparing to the ferroelectric capacitor used in the memory cell.

However, the larger size of ferroelectric capacitor in Fig. 3B is more influenced by the capacitor degradation. Thus, it is not reliable method.

Recently, a FeRAM of current gain cell having hierarchy bit line structure has been introduced for improving a data sensing margin.

However, there is not method introduced for optimal reference voltage by overcoming the above mentioned problems to be suitable to the FeRAM having the current gain cell mode.

5 Summary of the Invention

It is, therefore, an object of the present invention to provide a ferroelectric random access memory FeRAM for data sensing with simple peripheral circuit while constraining

10 variation of reference voltage caused by degradation of a ferroelectric capacitor by implementing an identical size of ferroelectric capacitor in a memory cell and a reference cell and different size of NMOS transistor as current gain transistor in a memory cell and a reference cell.

15 In accordance with an aspect of the present invention, there is provided a ferroelectric memory device, including: a memory cell unit having hierarchical bit-line structure formed by forming a word line and a plate line in a direction of a row and forming sub-bit line and main bit line in a direction

20 of crossing the word line and the plate line, and including a plural memory cells equipping a ferroelectric capacitor coupled to the sub bit line and a first current gain transistor having a gate coupled to the sub bit line, one end connected to a ground, and other end connected to the main bit

25 line; a reference cell unit having hierarchical bit line structure formed by forming a reference word line and reference plate line in a direction of a row and forming a

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reference sub bit line and a reference main bit line in a direction of crossing the reference word line and reference plate line, and including a reference cell quipping a ferroelectric capacitor coupled to the reference sub bit line

5 and a second current gain transistor having a gate connected to the reference sub bit line, an one end connected to a ground power supplying end and another end connected to the reference main bit line; and a sense amp unit for comparing voltages of the main bit line of the memory cell unit and the

10 reference main bit line of the reference cell unit, amplifying the voltage difference and outputting data, wherein a size of the two ferroelectric capacitor in the memory cell and the reference cell is identical and a size of the first current gain transistor and the second current gain transistor is

15 different.

Brief Description of the Drawing(s)

The above and other objects and features of the present

20 invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

Fig. 1 is a graph showing a characteristic of hysteresis loop of a conventional ferroelectric;

25 Fig. 2 is a circuit diagram illustrating a unit cell of conventional ferroelectric memory;

Figs. 3A and 3B are circuit diagrams showing a

conventional reference cell for generating a reference voltage in accordance with two different conventional methods;

Fig. 4 is a circuit diagram illustrating a FeRAM of current gain cell mode in accordance with a preferred embodiment of the present invention;

Fig. 5 is a circuit diagram of a reference cell unit in accordance with the present invention;

Fig. 6 is a graph showing a relation between the voltage of the sub bit line and a voltage of main bit line; and

Figs. 7A and 7B are graphs showing that optimal reference voltages generated according to a size of the current gain transistor in accordance with a preferred embodiment of the present invention.

Detailed Description of the Invention

Other objects and aspects of the invention will become apparent from the following description of the embodiments with reference to the accompanying drawings, which is set forth hereinafter.

Fig. 4 is a circuit diagram illustrating a FeRAM of current gain cell mode in accordance with a preferred embodiment of the present invention.

Referring to Fig. 4, the FeRAM of current gain cell mode includes a memory cell unit 420 having hierarchical bit line structure, a reference cell unit 440 for providing a reference voltage, and a sense amp unit 460 for outputting data by

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comparing a voltage of reference main bit line RMBL and a voltage of a main bit line MBL of the memory cell unit and amplifying a voltage difference.

The memory cell unit 420 has a hierarchical structure constructed by forming the word line WL and the plate line PL in a direction of row and forming the sub bit line SBL and main bit line MBL in direction of crossing the word line.

Also, the memory cell unit 420 includes a plural of memory cells 422 connected to the sub bit line SBL, a current gain transistor 424 having a gate connected to the sub bit line, a source (or drain) connected to a ground VSS, and a drain (or source) connected to the main bit line, and a main bit line sense load transistor 426 having a gate connected to the·VSS, a source (or drain) connected to the main bit line, and a drain (or source) connected to a power supplier Vcc.

A unit memory cell 422 includes a switching transistor TR having a gate connected to the word line and a drain connected to the sub bit line, and a ferroelectric capacitor having one end connected to the source of the transistor TR and other end connected to the plate line PL. A plural of the above mentioned unit memory cells 422 is connected to the sub bit line SBL to construct the memory cell unit 420.

.The reference cell unit 440 has a hierarchical bit line structure by forming a reference word line RWL and reference plate line RPL in a direction of row and forming a reference sub bit line and reference main bit line in a direction of crossing the reference word line RWL and the reference plate

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line.

Also, the reference cell unit 420 includes a plural of reference cells 442 connected to the reference bit line, a current gain transistor 444 having a gate connected to the reference sub bit line RSBL, a source (or drain) connected to a ground VSS and a drain (or source) connected to the reference main bit line and a reference main bit line sense load transistor 446 having a gate connected to the VSS, a source (or drain) connected to the reference main bit line RMBL and a drain (or source) connected to the Vcc.

The unit reference cell 422 includes a switching transistor TR having a gate connected to the reference word line RWL and a drain connected to reference sub bit line and a ferroelectric capacitor RFC having one end connected to a source of the transistor TR and another end connected to the reference plate line RPL. The reference cell unit 420 is constructed by connecting a plural of the above mentioned unit cells 422 to the reference sub bit line.

The current gain transistors 424 and 444 of the memory cell and the reference cell can be implemented by using NMOS and the sense load transistors 426 and 446 can be implemented by using a PMOS.

In the present invention, a size of the ferroelectric capacitor FC of the memory cell 422 and a size of the ferroelectric capacitor FC of the reference cell 442 are identical.

Also, in the present invention, a size of the current

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gain transistor 242 of the memory cell unit 420 and a size of the current gain transistor 424 of the reference cell unit 440 are different.

The present invention generates a mean voltage in the reference main bit line of a voltage $V_{RMBL"1"}$, which is corresponding to a logic "1" and a voltage $V_{RMBL"0"}$, which is a logic "0", as a reference voltage by controlling a size of the current gain transistor 424 of the reference cell unit 440. That is, the optimal reference voltage is generated by differently controlling a width and length of the current gain transistor 424 in the reference cell unit 440 comparing to the current gain transistor 424 in the memory cell unit 420.

Fig. 5 is a circuit diagram of a reference cell unit in accordance with the present invention.

Referring to Figs. 4 and 5, if a voltage is applied to the reference plate line RPL in the reference cell, a voltage of the reference sub bit line becomes the voltage $V_{RSBL"1"}$ corresponding to the logic "1" or the voltage $V_{RSBL"0"}$ corresponding to the logic "0" according to a state of storing data of the ferroelectric capacitor RFC.

A current flowing at the current gain transistor 444 is determined according to a voltage V_{RSBL} of the reference sub bit line and a voltage V_{RMBL} of the reference main bit line.

Since the reference main bit line is connected to the Vcc through PMOS, an amount of current flowing the load transistor 446 (PMOS) is determined by a size of the voltage V_{RMBL} of the reference main bit line. Since two current I_N and

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I_P are same in a parallel state, the voltage of reference main bit line is determined when the two current becomes same.

Fig. 6 is a graph showing a relation between the voltage of the sub bit line and a voltage of main bit line.

5 Referring to Fig. 6, a voltage of main bit line V_{MBL} is determined when the current I_N flowing at the current gain transistor and the current I_P flowing at the load transistor IP becomes identical.

For example, in a case that the sub bit line voltage
10 $V_{SBL"1"}$ is 1.8V when the ferroelectric capacitor is switched, the main bit line voltage $V_{MBL"1"}$ becomes 1.2V. Also, in a case that the sub bit line voltage $V_{SBL"0"}$ is 1.2V when the ferroelectric capacitor is non-switched, the main bit line voltage $V_{MBL"0"}$ becomes 2.7V.

15 Therefore, although a voltage difference ΔV_{SBL} of sub bit line voltages is 0.6V, a voltage difference ΔV_{MBL} of main bit line voltages is 1.5V. It clearly shows improvement of sensing margin, which is 2.5 times improved from the voltage difference ΔV_{SBL} of sub bit line voltages.

20 In here, a reference voltage V_{REF} between logic "1" and logic "0" is 1.9V, which becomes the optimal reference at 1.5V of V_{SBL}.

Figs. 7A and 7B are graphs showing that optimal reference voltages generated according to a size of the
25 current gain transistor in accordance with a preferred embodiment of the present invention.

An amount of current flowing the current gain transistor NMOS is increased in corresponding to increase of a width of the current gain transistor NMOS and is decreased in corresponding to increase of length of the current gain transistor NMOS.

Fig. 7A shows changes of reference voltage in a case of using non-switching charge of the ferroelectric capacitor by storing data '0' in the reference cell.

For gaining data showing in Fig. 7A, the current gain transistor 424 of Fig. 4 in the memory cell unit is set to a size of 0.6(width) x 0.3(length) and the current gain transistor 444 of Fig. 4 in the reference cell unit is set to a size of 1.2(width) x 0.3 (length). The graph of Fig. 7A shows that if sizes of the current gain transistors are set according to above mentioned, the optimal reference voltage V_{REF} is 1.9V.

Fig. 7B shows changes of reference voltage in a case of using a switching charge of the ferroelectric capacitor by storing data '1' in the reference cell.

For gaining data showing in Fig. 7A, the current gain transistor 424 of Fig. 4 in the memory cell unit is set to a size of 0.6(width) x 0.3(length) and the current gain transistor 444 of Fig. 4 in the reference cell unit is set to a size of 0.6(width) x 0.4 (length). The graph of Fig. 7A shows that if sizes of the current gain transistors are set according to above mentioned, the optimal reference voltage V_{REF} is 1.9V.

As mentioned above, the present invention can generate stable and exact reference voltage by controlling and implementing different size of NMOS transistors, which is easy to obtain characteristics and stable to manufacture, as current gain transistors in a memory cell and a reference cell. Therefore, it can reduce time and cost to optimize a size of a ferroelectric capacitor in order to generate the reference voltage in conventional method for manufacturing high integrated one transistor one capacitor (1T1C) ferroelectric random access memory (FeRAM).

The present invention can increase a lifetime and reliability of FeRAM by constraining variation of reference signal caused by degradation comparing to a method using a signal corresponding to data '0' of a ferroelectric capacitor, which is much larger than a ferroelectric capacitor in a memory cell, as the reference signal.

The present invention can generate a reference signal by using only one cell instead of using a mean value of data 1 and data 0 in the conventional method. Therefore, the present invention requires simple circuit for generating the reference signal and it is convenience to generate the reference signal.

While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.